Whitepaper:

3D Integrated Circuits

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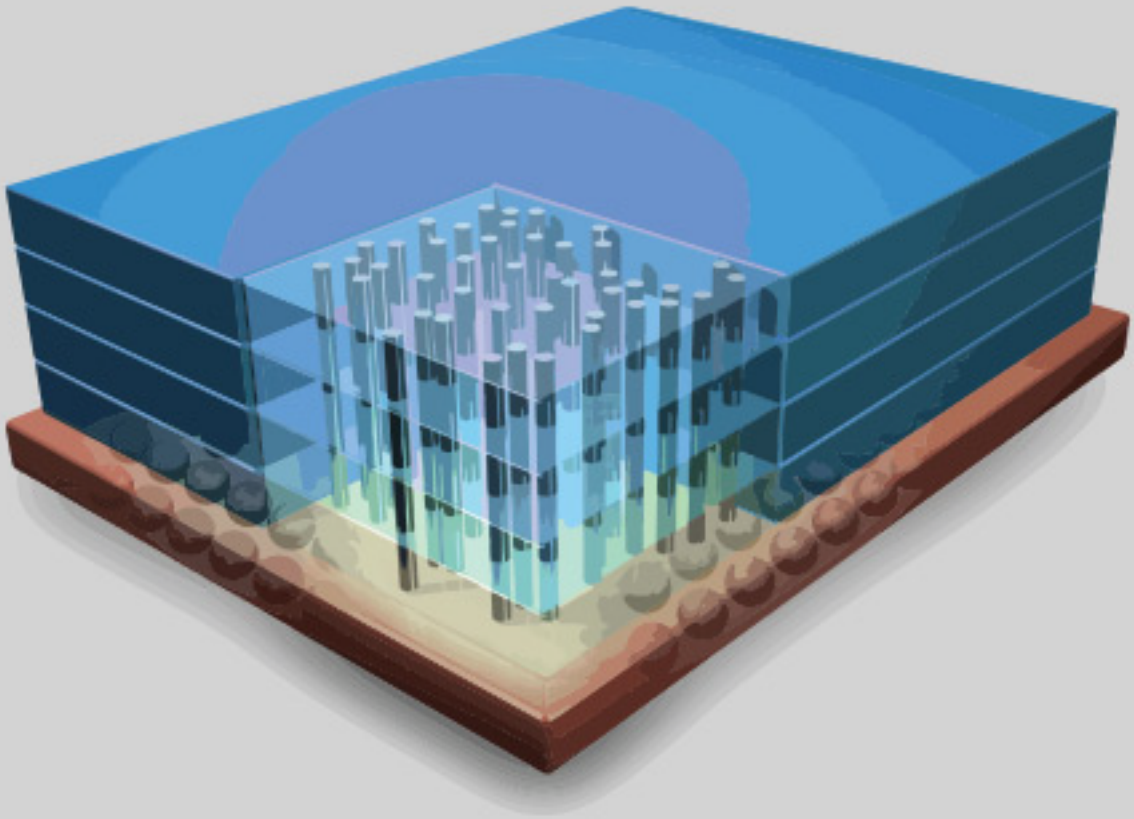

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01. Introduction

In the semiconductor world, a new trend has emerged to vertically stack homogeneous or heterogeneous dies or integrated circuits (ICs) into Multi-Chip-Module (MCM) with Through-Silicon-Via (TSV).

TSV is a platform for mono- or multi-functional integration. It can accommodate 2, 4, or 8 memories into one single package. Further, it is also possible in the future that the CPU, GPU, DRAM and main-broad could be all shrunk into one single package.

3D IC is a solution of high bandwidth, small form factor, and multi-function integration.

It is the proper solution for meeting the requirements of electronic devices like better performance, high functionality, less power consumption, and a smaller footprint.

The different methods used for this purpose are known as **3D integration technologies.**

Overall, 3D integration is a broad term, and it includes technologies such as:

- 3D wafer-level packaging
- 2.5D and 3D interposer-based integration
- 3D stacked ICs (3D-SICs), monolithic 3D ICs
- 3D heterogeneous integration; and 3D systems integration

Below are the advantages of 3D ICs:

Drivers of 3D Integration Technology

Increasing demands for advanced electronic products with which consist of a smaller form factor and has superior functionality.

High demand for 3D packaging using TSVs driving 3D IC development advanced packaging technologies.

High adoption of fan-out wafer level packaging technology.

There are also some challenges faced in the adoption of 3D ICs:

Cost

While cost is a benefit when compared with scaling, it has also been identified as a challenge to the commercialization of 3D ICs in mainstream consumer applications.

Heat

Heat building up within the stack must be dissipated. This is an inevitable issue as electrical proximity correlates with thermal proximity. Specific thermal hotspots must be more carefully managed

Design Complexity

Taking full advantage of 3D integration requires sophisticated design techniques and new CAD tools.

Testing

To achieve high overall yield and reduce costs, separate testing of independent dies is essential. However, tight integration between adjacent active layers in 3D ICs entails a significant amount of interconnect between different sections of the same circuit module that were partitioned to different dies.

Lack of Standards

There are few standards for TSV-based 3D IC design, manufacturing, and packaging, although this issue is being addressed. In addition, there are many integration options being explored such as via-last, via-first, via-middle; interposers or direct bonding; etc.

Heterogeneous Integration Supply Chain

In heterogeneously integrated systems, the delay of one part from one of the different parts suppliers delays the delivery of the whole product, and so delays the revenue for each of the 3D IC part suppliers.

Lack of Clearly Defined Ownership

It is unclear who should own the 3D IC integration and packaging/assembly. It could be assembly houses like ASE or the product OEMs.

02. Manufacturing/Fabrication Technologies for 3D ICs

There are various ways for 3D IC design, which include recrystallization and wafer bonding methods. Two major types of wafer bonding include:

Cu-Cu connections (copper-to-copper connections between stacked ICs, used in TSVs) and

Through-silicon via (TSV)

There are multiple key stacking approaches, including die-to-die, die-to-wafer, and wafer-to-wafer.

Die-to-Die

Electronic components are built on multiple die, which are then aligned and bonded. Thinning and TSV creation may be done before or after bonding. One advantage of die-to-die is that each component die can be tested first, so that one bad die does not ruin an entire stack.

Moreover, each die in the 3D IC can be binned beforehand, so that they can be mixed and matched to optimize power consumption and performance (e.g. matching multiple dice from the low power process corner for a mobile application).

Die-to-Wafer

Electronic components are built on two semiconductor wafers. One wafer is diced; the singulated dice are aligned and bonded onto die sites of the second wafer. As in the wafer-on-wafer method, thinning and TSV creation are performed either before or after bonding. Additional die may be added to the stacks before dicing.

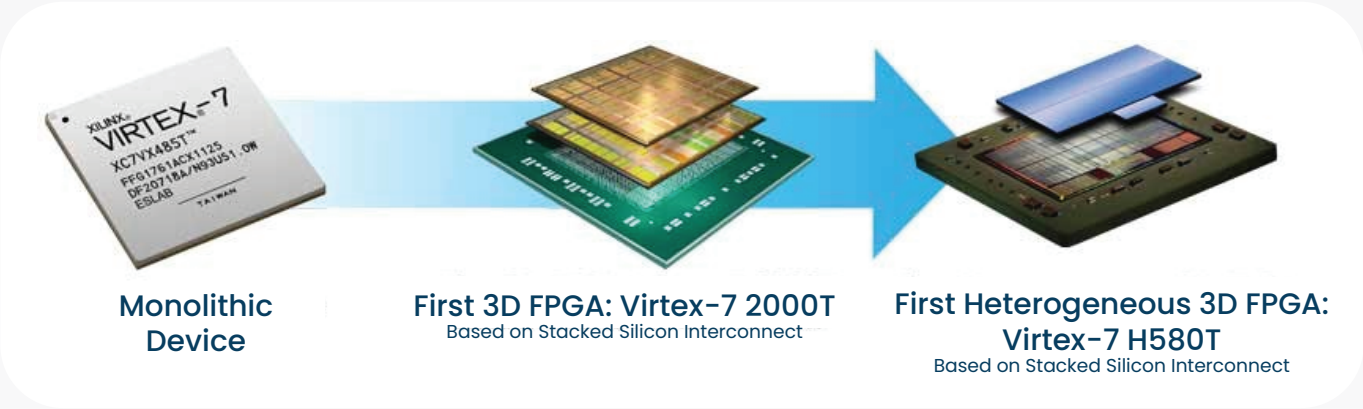
Wafer-to-Wafer

Vertical connections are either built into the wafers before bonding or else created in the stack after bonding. TSVs pass through the silicon substrates between active layers and/or between an active layer and an external bond pad. Wafer-to-wafer bonding can reduce yields, since if any 1 of N chips in a 3D IC are defective, the entire 3D IC will be defective. Moreover, the wafers must be the same size, but many exotic materials are manufactured on much smaller wafers than CMOS logic or DRAM, complicating heterogeneous integration.

03. Top Players and Their Products

a. Xilinx

Xilinx 3D ICs take leverages of the technology called stacked silicon interconnect (SSI) to overcome the shortcomings of Moore's law and provide the capabilities to fulfill the most demanding design needs. Xilinx homogeneous and heterogeneous 3D ICs deliver the highest logic density, bandwidth, and on-chip resources in the industry, breaking new ground in system-level integration.



Two major technologies used in Xilinx 3D IC's are described below

UltraScale Architecture

Xilinx Ultrascale 3D ICs provide high levels of system integration,performance, bandwidth, and capability.

Both Virtex ultrascale 3d ICs and Xilinx Ultrascale 3D ICs consists of a step-function increase in both the amount of connectivity resources and the associated interdie bandwidth in this second-generation 3D IC architecture.

The Big increase in routing and bandwidhth and the new 3D IC wide memory optimized interface ensured that next-generation applications can achieve their target performance at extreme levels of ultilization. Virtex Ultrascale 3D+ ICs includes all of the architectural innovations delivered with Ultrascale families and incorporate 16nm 3D transistors for a '3D-on-3D' step function increase in performance per watt, with optional HBM memory.

SSI Technology

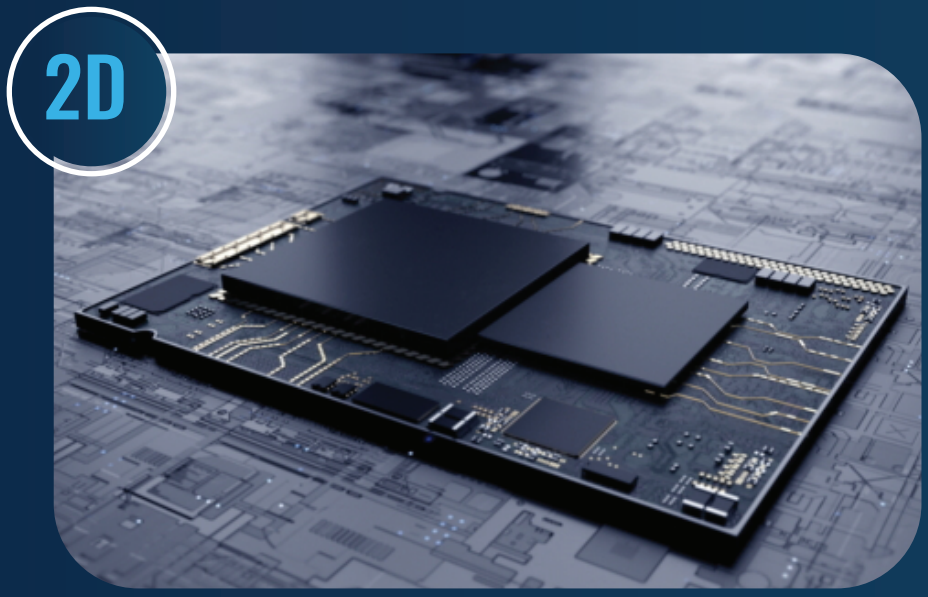
SSI is a well-known technology and is used in Versal HBM series, Versal Premium series, Virtex UltraScale+, Virtex UltraScale, Kirtex UltraScale, and Virtex -7 families thereby offering customers a broad range of resources and capabilties to match leading edge demands. The SSI devices shown below offer unprecedented FPGA capabilities and are ideal for applications such as next-generation wired communications,high-performance computing, and ASIC prototyping/emulation.

b. Samsung

• Samsung has introduced a new technology, called X-Cube, which was tested and proven in a 7nm test chip, which assembled SRAM on top of a logic chip. The output result was a smaller footprint and shorter signal paths, leading to faster signal propagation and less power consumption. It is also available in advanced nodes: both 7nm and 5nm.

• This technology focuses on several trends in chip design: the end of Moore's law, increased chip functionality, and solves the difficulties of systems-on-chip (SoCs).

•X-Cube is enabled by 3D integration; the ultra-thin package design features very short signal paths between the dies for maximized data transfer speed and energy efficiency. Customers can also scale the memory bandwidth and density as per their desired specifications.



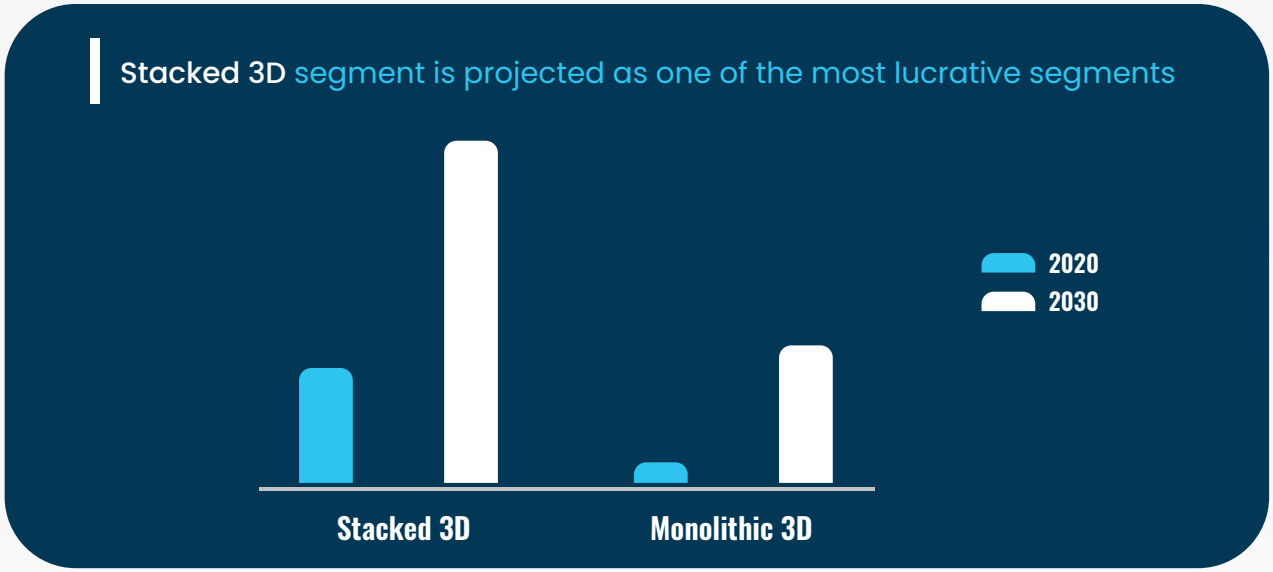
04. Market Analysis

Forecast:

The expected growth of the 3D IC market may be $51.81 Billion by 2030, growing at a CAGR of 20% from 2021 to 2030.

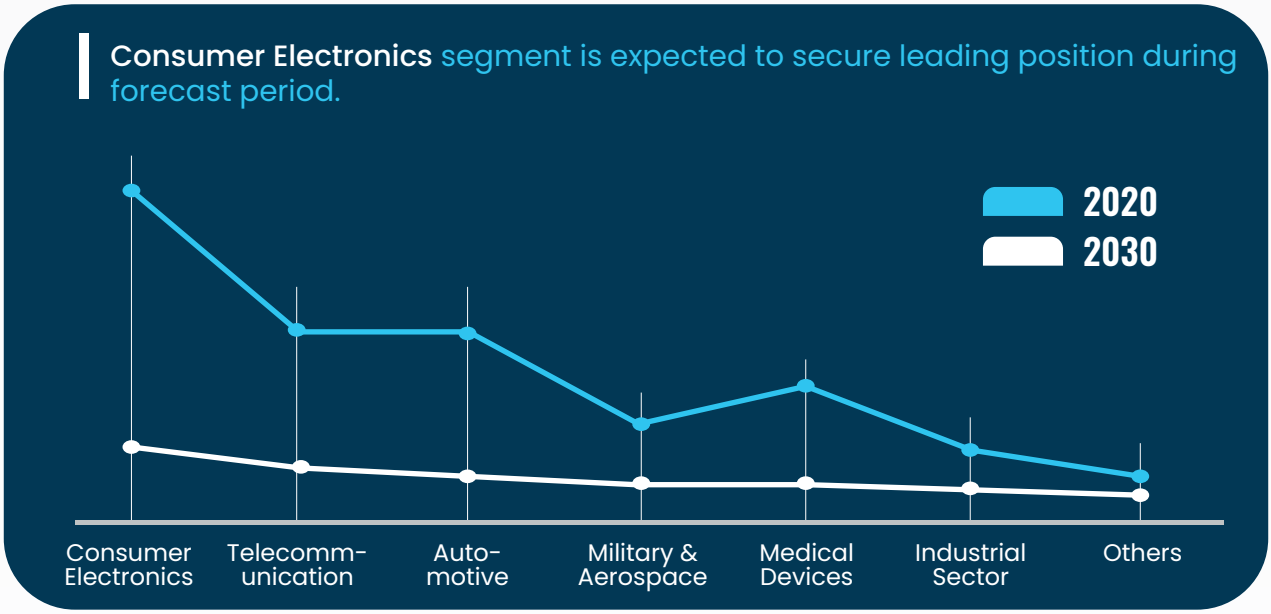
Based on the type of 3D IC, what the market may look like is displayed in the graph below:

3D IC market
By Type

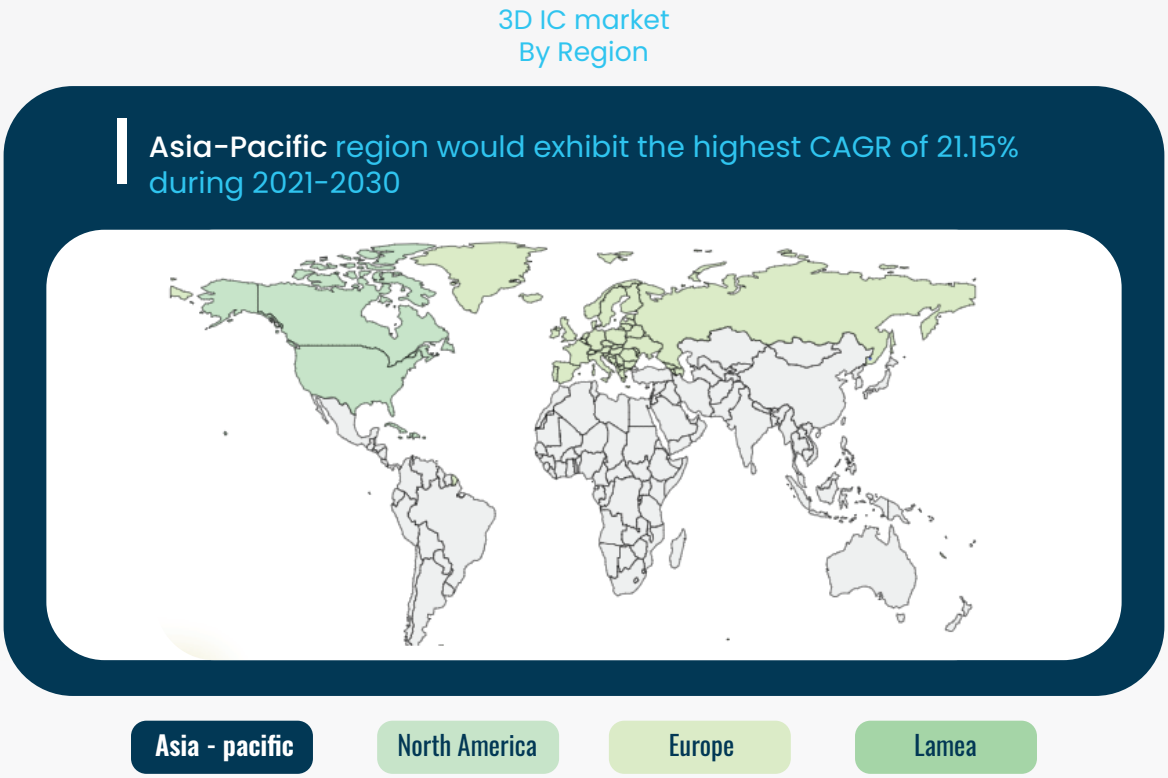


The main factors for the growth of the 3D IC market include high adoption of electronics devices, increase in request for internet of things (IoT) technology, and technological advancement in 3D packaging technology. On the opposite side, high initial capital investment and high cost of materials are barriers to its adoption, which are expected to be the major threat to global market growth. Combining all these factors together, the 3D IC market is divided based on the end consumer.

3D IC market
By End User



Another criterion based on which the 3D IC market is divided is region:



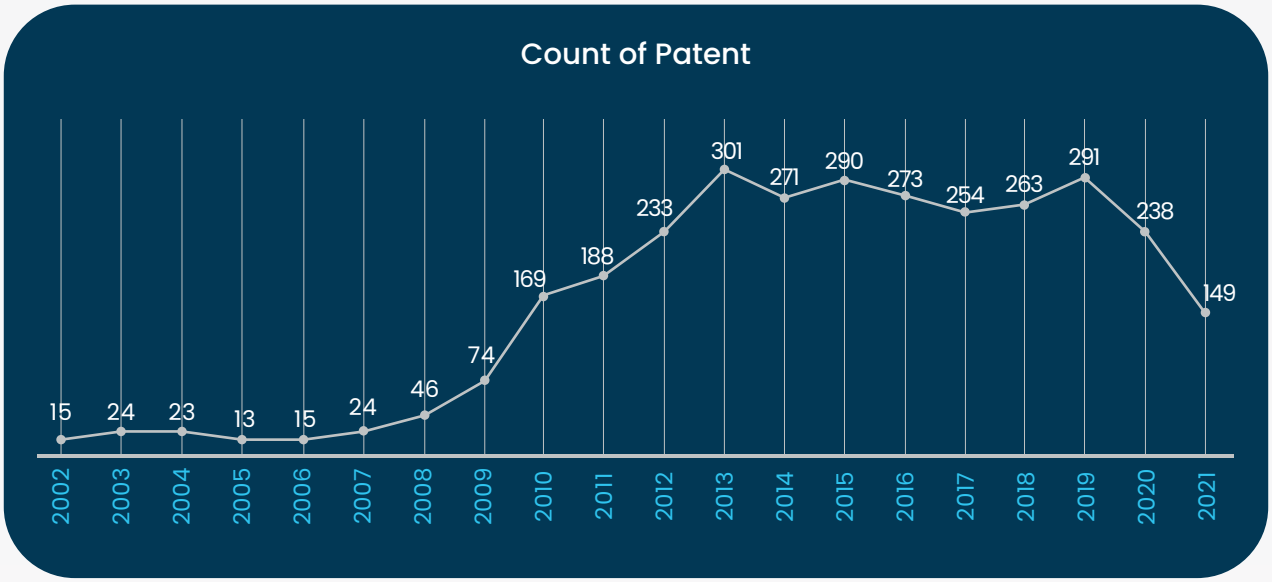
05. Patent Trends

a. Application Year-Wise Patent Trend:

3D ICs were first demonstrated in 1980s in Japan fabricated with a through-silicon via (TSV) process. The most common form of 3D IC design is wafer bonding.

Hitachi filed a Japanese patent in 1983, followed by Fujitsu in 1984. In 1986, a Japanese patent filed by Fujitsu described a stacked chip structure using TSV.

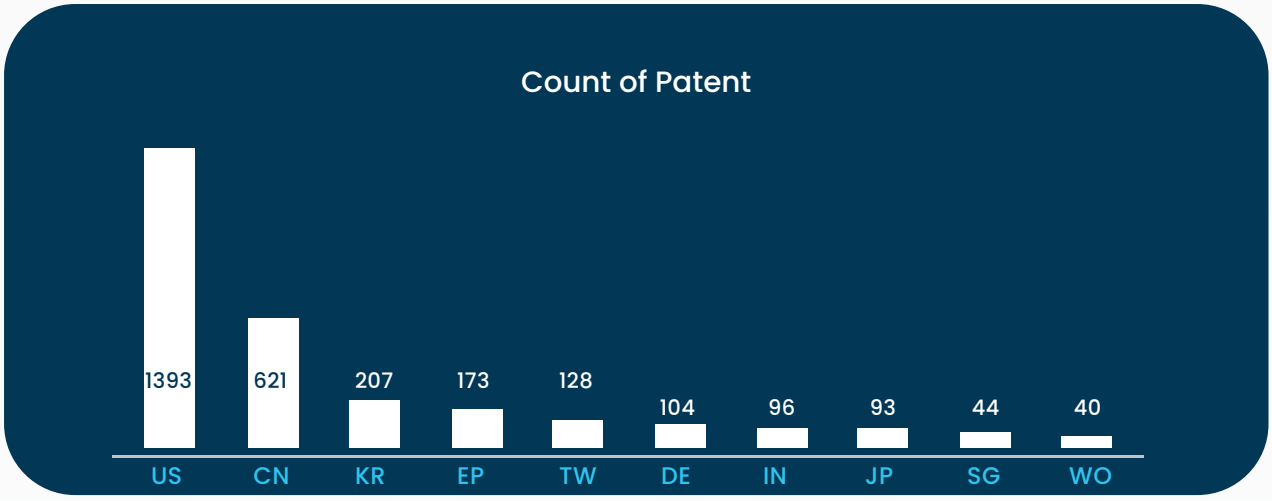
Thereafter, a number of patents have been filed related to 3D integrated circuits. The patent trends of the last 20 years can be viewed from the graph below:



As can be seen from the graph, the patent filing trend has increased after 2008 was almost consistent between 2012 to 2020. The maximum number of patents were filed in 2013 (301 patents).

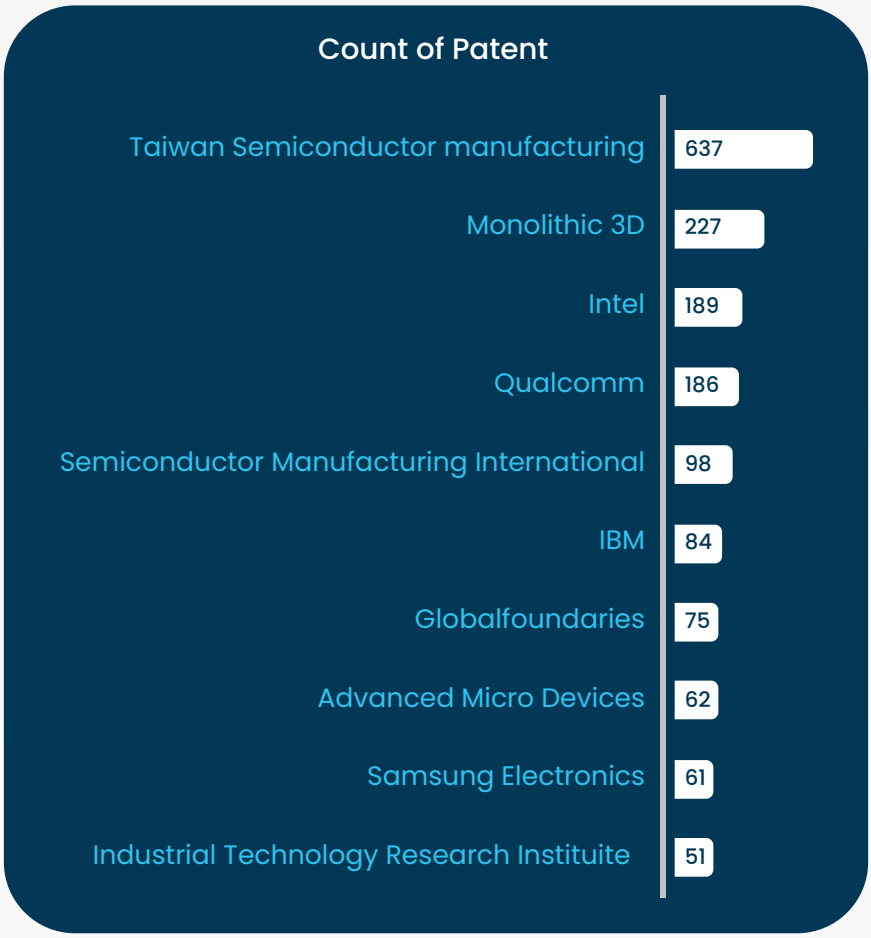
b. Country-Wise Patent Trend:

Based on the country of protection, **patent distribution** in 3D IC technologies can be seen from the graph below:



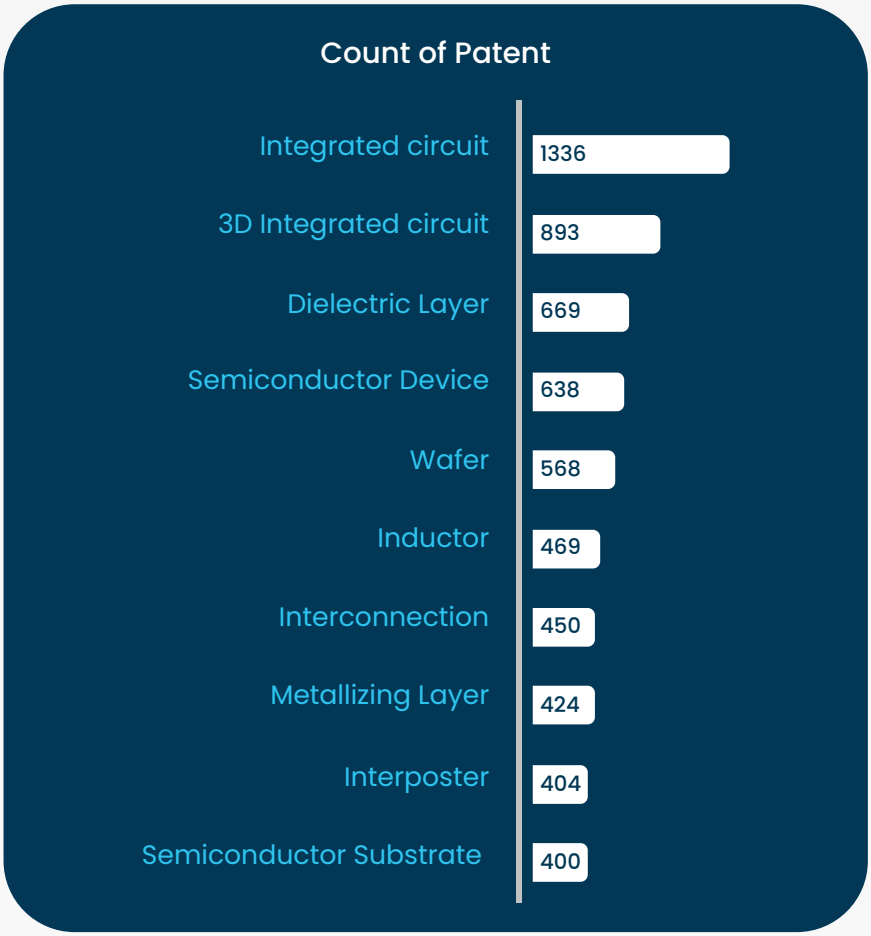
c. Top Assignee-Wise Patent Trend:

Top 10 players who have filed maximum patents in the 3D IC fabrication are shown in the graph below:



d. Technology-Wise Patent Trend:

The graph below represents the technology concepts under which maximum number of patents are filed related to 3D integrated circuits.



06. Conclusion

With the end of Moore's law, and the ever-increasing demand of compact chips, 3D Integrated Chips have come up as a potential solution to fulfill the requirement.

3D ICs are very small in size, which reduces the weight and cost of the overall electronic product. Due to the absence of soldered connection, few interconnections, and a small temperature rise, failure rate is low. Hence, it is highly reliable. The smaller the size, lesser the power consumption, and it can be easily replaced in the event of failure.

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