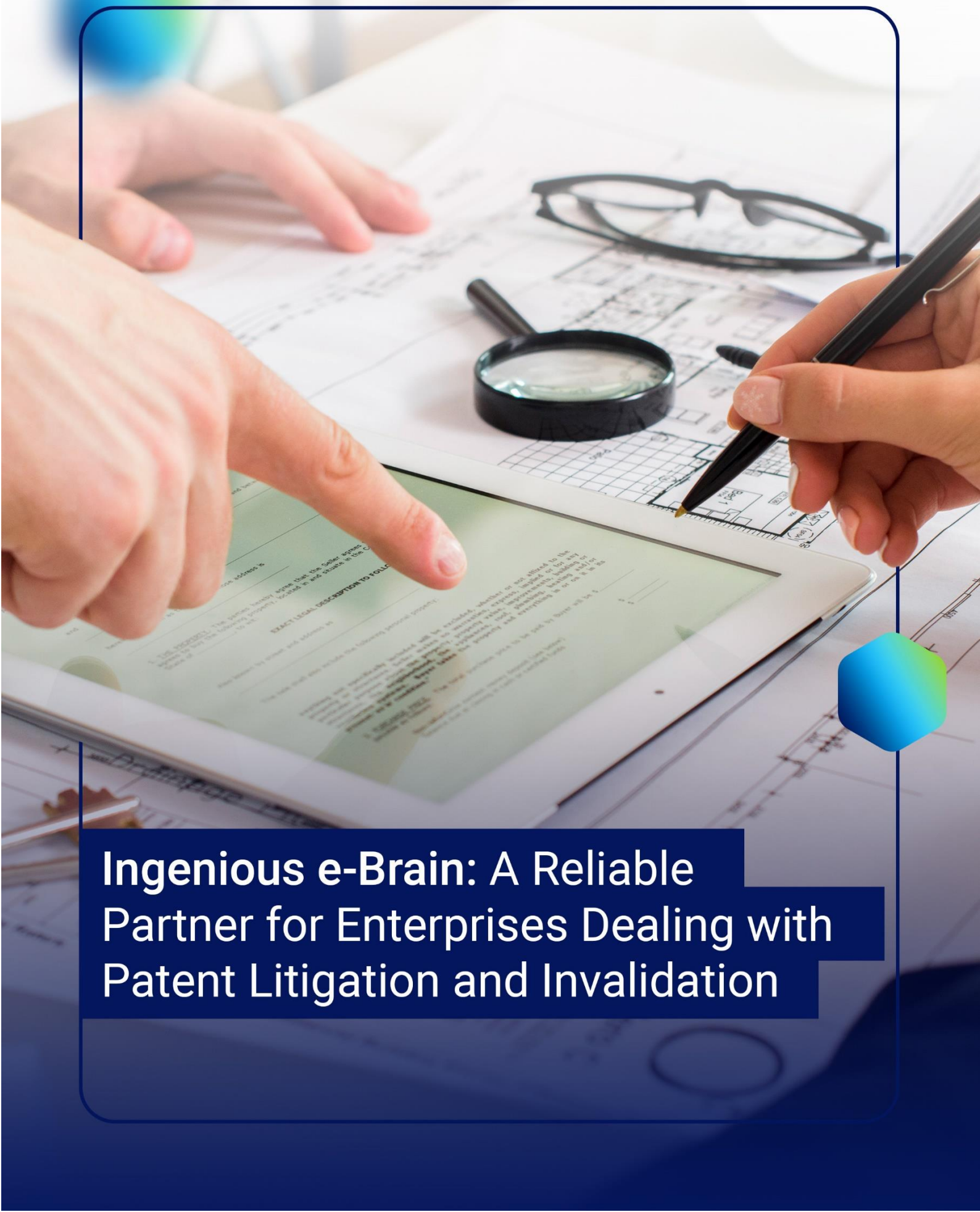
Ingenious e Brain



Ingenious e-Brain: A Reliable Partner for Enterprises Dealing with Patent Litigation and Invalidation

Before delving into the key reasons that make us an apt supporter, let's first understand the need for invalidation or opposition search …

An invalidation study is used to analyze the closest prior art results before the priority date with respect to the claims of the subject patent, thereby invalidating or revoking an already registered/ granted patent claim or for a pre-grant opposition of a published patent application claim.

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- ✓ We provide both novelty and inventiveness-based search strategies to kill an art
- ✓ We follow KSR Seven Rationales for determining the obviousness
- ✓ We deliver high-definition color-coded claim charts to reduce attorney efforts in review
- ✓ We generate a feature matrix for each feature to quickly review the report
- ✓ We have access to paid non-patent databases, such as IEEE, Scopus, Web of Science, etc.
- ✓ We provide the classification data of patents translated into Japanese & Korean languages
- ✓ We categorize results as per the International Search Report (ISR) standard
- ✓ We conduct standard searches on 3GPP & IEEE portal
- ✓ We have proven records of associating with and supporting Fortune 500 companies

Some Snippets from IeB Research Documents

- **High-definition Color coded charts with analyst's comments**

#	Claims	Description	Comment on Comparison	Comparison Result
1.	**Claim 1** A method of manufacturing a printed wiring board having at least one solder bump thereon, the method comprising:	**[Summary of the Invention, Column 3, Line 0035 – 0050]** In order to achieve the above objects according to the present invention, a method is provided for evaluating configuration of solder external terminals of a **BGA-type tape-based semiconductor device mounted on** a mounting board such that the external terminals are joined to lands provided on the mounting board, the method including the steps of: a) obtaining geometric data related to openings of a tape substrate of the semiconductor device, **solder balls to be placed** at positions corresponding to the openings, and the lands of the mounting board; and b) deriving configuration of the solder external terminal based on the geometric data. With the invention described above, since the estimation is based on known geometric data of the tape openings, **solder balls** and the lands, the configuration of the solder external terminals can be evaluated without actually mounting **the solder balls** on the mounting board. Accordingly, the solder balls can be evaluated accurately and with reduced time.	In reference to the embodiment Semiconductor device is being used including solder balls	supported
2.	forming a solder resist layer on a conductor layer, the solder resist layer having at least one opening that exposes a connection pad of the conductor layer,	**[Description of related Art, Column 1, Line 0040 – 0060]** FIG. 1 is a Schematic diagram showing a Semiconductor device 1 having a package Structure of a FBGA type. The Semiconductor device 1 generally comprises a tape 2, a Semiconductor chip 4, ball-shape Solder external terminals 6 and a Sealing resin 8. **The tape 2 is made of a material Such as polyimide resin. Electrode patterns 10** and bonding pads 12 are provided on a first (upper) Surface 2a of **the tape 2.** Also, the Semiconductor chip 4 is mounted on the first Surface 2a of the tape 2. In order to **provide the electrode patterns 10** and the bonding pads 12, **a copper layer is formed on tape 2** and then an etching process is implemented on the copper layer to form predetermined patterns. **The electrode patterns 10** and the bonding pads 12 are electrically connected by wiring patterns(not shown). Also, wires 14 are provided between the semiconductor chop 4 and the bonding pads 12. Accordingly, the semiconductor chip 4 and the electrode patterns 10 are electrically connected via the wires 14, the bonding pads 12 and the wiring patterns. **Further tape opening 16 are formed through the tape 2 at positions corresponding to the electrode patterns 10 of the tape 2.**	Tape 2 made of polyimide resin which is considered as solder resist layer on electrode plate	Supported

FIG. 1

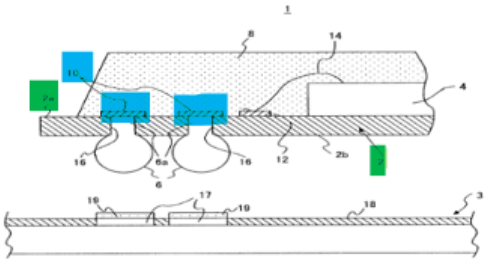
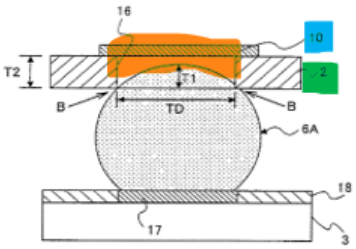


FIG. 7



- **Key feature matrix with clear indications regarding partially and inferentially disclosed features**

LEGAL STATUS	Granted	Pending	Lapsed	Expired

#	Key features	Colour represents inferentially (I) /partially (P) supported					
		WO2018146661A2	KR10106579781	US7637040B2	FR2897517A1	CN113106720B	CN103422334A
1	An ironing device comprising:	✓	✓	✓	✓	✓	✓
1(a)	a glove configured to be worn on a user's hand and including at least one contact portion configured to be placed in contact with a garment,	✓	✓	✓	✓	✓	✓
1(b)	ironing means that are integral with said glove and arranged at least along said contact portion	✓	✓	I	✓	P	✓
1(c)	control means operatively connected to said ironing means and configured to control the operation of said ironing means, and characterised in that	✓	✓	✓	✗	I	✗

Symbols	Definition
✓	Fully supported: - The patent reference supports all the elements of the subject patent claims
I	Inferentially supported: - The patent reference has disclosed a broad concept and does not explicitly disclose the certain concept as disclosed in the subject patent
P	Partially supported: - The patent reference has disclosed certain elements of the subject patent claim and has not revealed some other parts of that claim
✗	Not supported: Key Feature not found

- **Category-wise segregation of findings**

1.1 List of Patent Results

1.1.1 Tier-I (Category X)

#	Publication Number	Title	Associated Patent Law	Publication Date	Filing Date	Priority Date	Assignee(s)	Inventor
1.	JPXXXXXXXXX9A	POWER TOOL	35 U.S.C. 102 (b)	September 18, 2008	March 1, 2007	March 1, 2007	PANASONIC	Sunao Arimura et al.
2.	JPXXXXXXXXX8A	POWER TOOL	35 U.S.C. 102 (a)	April 7, 2011	September 25, 2009	September 25, 2009	PANASONIC	Hiroshi Miyazaki et al.
3.	JPXXXXXXXXX7A	COMMUNICATION SYSTEM AND METHOD FOR IMPLEMENTING COMMUNICATION THROUGH ELECTRIC SUPPLY TERMINAL IN DIRECT CURRENT POWER TOOL	35 U.S.C. 102 (b)	August 11, 2005	January 31, 2005	January 30, 2004	BLACK & DECKER	Daniele C Brotto et al.

1.1.2 Tier-II (Category Y)

#	Publication Number	Title	Associated Patent Law	Publication Date	Filing Date	Priority Date	Assignee(s)	Inventor
1.	JPXXXXXXXXX9A	BATTERY PACK AND ADAPTER	35 U.S.C. 102 (b)	August 1, 2007	March 1, 2001	March 1, 2001	MAKITA	Hirokatsu Yamamoto

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INDIA (HQ)

Unit 207-208, 2nd Floor, Welldone Tech Park Sohna Road, Sector 48, Gurugram, Haryana 122018

Phone No. - **+91 124 429 4218**

USA

646 Sutton Way #1006 Grass Valley, United States CA 95945

Phone No. - **+1 347 480 2054**

UK

13 Freeland Park, Poole, Dorset, United Kingdom, BH16 6FH

Phone - **+ 44 207 193 3548**